PAPER ID-311379

Subject Code: KCA105

Roll No: | | | | | | | | | | | | | |

MCA

(SEM I) THEORY EXAMINATION 2023-24

COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Let M = 11111010 and N = 00001010 be two 8-bit two's compliment number. Their product in two's complement is ----------.	2	1
b.	Differentiate between clock cycles and clock frequency.	2	1
c.	Explain the role of program counter.	2	2
d.	A bulb in a staircase has two switches, one switch being on the ground floor and the other one on the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches, irrespective of the state of the other switch. The logic of switching of the bulb resembles to which gate.	2	2
e.	Describe any four status bits in detail by taking suitable example.	2	3
f.	Discuss the concept of PSW.	2	3
g.	Differentiate between write back and write through in cache memory.	2	4
h.	Differentiate between SRAM and DRAM.	2	4
i.	Explain maskable and non-maskable interrupt.	2	5
j.	Distinguish between burst transfer and cycle stealing method.	2	5

SECTION B

2. Attempt any *three* of the following:

a.	Explain the function of control unit in general register organization with the help of diagram.	10	1
b.	Describe BOOTH multiplication algorithm and Multiply (-13) x (-21) and draw the flowchart of Booth's algorithm.	10	2
c.	Show the block diagram of microprogram sequencer. Consider a microprogrammed CU, where 1024-word control memory is used. The CU has to support 40 control signals and 32 flag conditions. How many bits are required in the control word? What is the size of horizontal and vertical control memory	10	3
d.	A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. 1. How many bits are required for addressing the main memory? 2. How many bits are needed to represent the TAG, SET and WORD fields?	10	4
e.	Outline the block diagram of DMA controller. Illustrate, why are the read and write control lines in a DMA controller bidirectional?	10	5

SECTION C

3. Attempt any *one* part of the following:

a.	**I**llustrate a BUS system? Implement a BUS of 4 lines with MUX.	10	1
b.	Demonstrate the concept of addressing modes. The instruction is stored at location 700 with its address fields at location 701. The address field has the value 1000. A processor register contains the value 500 and index register	10	1

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	contains the value 300. Evaluate the effective address if the addressing mode of the instruction is (a) Direct (b) Indirect (c) Immediate (d) Relative (e) Register Indirect (f) Autoincrement (g) Autodecrement		

4. Attempt any *one* part of the following:

a.	Explain the concept of 4-bit fast adder in detail along with neat & clean diagram.	10	2
b.	Perform the division process of 00001111 by 0011 using division restore method.	10	2

5. Attempt any *one* part of the following:

a.	Determine a program to evaluate the arithmetic statement. X = (A*B-C) / (D+E/F) • Using general register computer with 3-address instruction. • Using general register computer with 2-address instruction. • Using an accumulator type computer with 1-address instruction. • Using a stack organized computer with 0-address instruction	10	3
b.	Compare horizontal microprogramming and vertical microprogramming. The microprogrammed control unit has a control memory of 1024 words of 32 bits each. The micro construction has three fields, and the micro-operations field has 16 bits. a. How many bits are there in the branch address field and the select field? b. If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bit? c. How many bits are left to select an input for the multiplexers.	10	3

6. Attempt any *one* part of the following:

a.	Examine the following organizations of cache memory: (i). Associative mapping (ii). Direct Mapping (iii). Set associative mapping. Consider memory block request: 3, 4, 8, 3, 9, 6, 16, 13, 35, 12, 3, 8, 6, 7, 30, 45, 12, 67, 22. Consider a full associative mapping for the 8 cache blocks find the following values for LRU and FIFO • Number of miss and Number of hits • Hit ratio. • Cache block number which contains main memory block 6	10	4
b.	A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. Then find the number of bits available for the immediate operand field.	10	4

7. Attempt any *one* part of the following:

a.	Describe asynchronous data transfer? What are the methods through which it can be achieved?	10	5
b.	Discuss the modes of transfer & explain the following. (i) Programmed I/O (ii) Interrupt initiated I/O	10	5