Printed Pages : 1 **Roll No.** | | | | | | | | | | | **NEC042**

B. TECH.

THEORY EXAMINATION (SEM–VIII) 2016-17

DIGITAL SYSTEM DESIGN USING VHDL

Time : 3 Hours ***Max. Marks : 100***

Note : *Be precise in your answer. In case of numerical problem assume data wherever not provided.*

SECTION-A

1 Explain the following: **(10×2=20)**

a. Generics.
b. Concurrent statements and Sequential statements.
c. Array and Records types.
d. Function and Procedure.
e. Packages and Library.
f. Process and Wait statement.
g. Conditional and Case statement.
h. Structural Modelling.
i. Transport and Delta Delay.
j. HDL design flow for synthesis.

SECTION-B

2 Attempt any five of the following: **(10×5=50)**

a. Draw block diagram for UART and SM chart for UART transmitter and discuss the VHDL code for UART transmitter.
b. What is the various floating operation? Draw and explain the flow chart for floating point multiplication.
c. Write a high level VHDL description of the divider.
d. Write a short note on synthesis of VHDL codes.
e. Draw a state graph for 4x4 binary multiplier control and discuss the behavioral VHDL model.
f. Using block diagram explain compilation elaboration and simulation of VHDL code. Write a VHDL description of an SR latch use two logic gates.
g. Write a VHDL code for a full subtractor using logic equation.

SECTION-C

Attempt any two of the following: **(15×2=30)**

3. Write down the truth table, working of a 16 x 1 multiplexer along with its diagram. Implement 16 x 1 multiplexer in VHDL using case statement with suitable diagram.

4. Write down the VHDL code for ALU and describe it's working. Briefly explain the function of control unit with suitable diagram.

5. Write short note on the followings with suitable diagram:

a. FPGA.
b. CPLD
c. PLA and PAL