Printed Pages : 1 **Roll No.** | | | | | | | | | | | **NEN021**

B.TECH.
THEORY EXAMINATION (SEM–VI) 2016-17
VLSI DESIGN

Time : 3 Hours ***Max. Marks : 100***

Note : *Be precise in your answer. In case of numerical problem assume data wherever not provided.*

SECTION – A

1. Explain the following: **10 x 2 = 20**

(a) Why silicon is preferred over germanium? Explain.
(b) Define LSI, MSI, VLSI, and ULSI on number of transistor basis?
(c) Define testing?
(d) Why scaling has a great importance in VLSI circuits?
(e) What are the three main domain of design?
(f) Differentiate between static logic circuits and dynamic logic circuits?
(g) What are needs for low power VLSI chips?
(h) Classify semiconductor memories
(i) What is a twin-well process?
(j) What are the major drawbacks of pass transistor logic?

SECTION – B

2. Attempt any five of the following questions: **5 x 10 = 50**

(a) Explain the issues involved in BIST testing?
(b) Describe the stick layout design style for CMOS circuit design?
(c) Draw a CMOS inverter and explain its transfer characteristics?
(d) Define transconductance and output conductance of MOS transistor. Also find expression for Transconductance?
(e) What are FPGAs? Discuss the salient features of FPGAs
(f) Explain read/write operation of SRAM memory cell.
(g) With a neat sketch of cross section of n-channel depletion type MOS transistor, explain the operation and draw the V-I characteristics of the device?
(h) Describe the polysilicon gate self-aligning NMOS fabrication process?

SECTION – C

Attempt any two of the following questions: **2 x 15 = 30**

3. What are the different types of faults in logic circuits? How is the logic gates tested for stuck-at-fault?

4. Discuss a combined voltage and dimension scaling model. Compare the scaling factors for the following device parameters: Gate area, Gate capacitance, channel resistance, current density and power dissipation for the different scaling models.

5. What are the important parameters of good VLSI design? Enlist the various design techniques and explain fully the cell based design technique.