ORGANIZING COMMITTEE

Chief Patron:

His Holiness Jagadguru Sri Shivarathri Deshikendra Mahaswamigalavaru
President, JSS Mahavidyapeetha, Mysuru

Patrons:

Prof. Vinay Kumar Pathak, Vice chancellor, AKTU, Lucknow
Dr. C.G Betsurmath, Executive Secretary, JSSMVP, Mysuru
Prof. M. H. Dhananjaya, Advisor, Technical Education Division,JSSMVP, Mysuru
Dr. C. Ranganathaiah, Director (Academic & Administration),JSSMVP, Mysuru
Dr. B.G. Sangameswara, Vice Chancellor, JSS S&TU, Mysuru

General Chair:

Prof. H.K. Paliwal, Dean of faculty, AKTU, Lucknow.
Dr. B.K. Murthy, Scientist G and Group Coordinator, MeitY, Govt. of India.
Prof. T. N. Nagabhushan, Principal, JSS S&TU, Mysuru.
Dr. Arti Noor, Joint Director, C-DAC, Noida.
Prof. V.K. Singh, BOS Convenor, AKTU, Lucknow.
Prof. J.P. Saini, Director, NSIT, New Delhi.
Prof. J.P. Pandey, Director, KNIT, Sultanpur.
Dr.Vineet Kansal, Dean(UGSE) and TEQIP-III Coordinator,AKTU,Lucknow.

Program Chair:

Prof. G.M.Patil, Principal, JSSATE, Noida.

Program Coordinator:

Prof. Sampath Kumar V., Head of Department,
Department of Electronics & Communication Engineering, JSSATE, Noida and Associate Dean (RDIC), AKTU, Lucknow.

Departmental Organizing Committee:

Ms. Rashika Anurag,Assistant Professor, JSSATE, Noida. (9871644060)
Mr. Ganesha H.S., Assistant Professor, JSSATE, Noida. (9964944390)

REGISTRATION DETAILS

Those willing to attend this FDP should send filled registration form to ecworkshop@jssaten.ac.in. Registration is free and will be on a first-come-first-serve basis. Confirmation of registration will be informed by email. Accommodation and TA / DA will not be provided.

LAST DATE OF REGISTRATION

10th August, 2018

Technical Education Quality Improvement Programme-Phase III

Dr. A.P.J Abdul Kalam Technical University, Lucknow

Faculty Development Program On

Analog Integrated Circuit Design using Cadence Analog Design Flow

27 th August– 1st September, 2018

INDUSTRY PARTNERS

Texas Instruments, Synopsys, ST life.augmented, Cadence, Entuple Technologies, NXP, NMTRONICS

VENUE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
JSS ACADEMY OF TECHNICAL EDUCATION
C-20/1, Sector 62, Noida. Ph: +91-0120-2400115 www.jssaten.ac.in

ABOUT THE COLLEGE

JSS Academy of Technical Education Noida (JSSATEN) is one of the leading Technical Institutions in the National Capital Region in the State of Uttar Pradesh. Established in the year 1998 by JSS Mahavidyapeetha, Noida, the Institution has set benchmarks every year, and grown into an Institution of Excellence in Technical Education. Located in the central part of NOIDA, JSSATEN has become a household name for its excellence in Discipline, Teaching, Training and Placement. The Institution has MOUs with Colorado Heights University, Denver, USA for student exchange program. IBM Centre of Excellence, Texas Instruments Centre of Excellence, Nokia Mobile Innovation Labs, e-Yantra - Embedded & Robotics Lab funded by MHRD under NMEICT, PLMCC, Schneider Electric Substation Automation Labs and Centre for Innovation & Design are additional facilities for the students to innovate new ideas. JSSATEN is proud to mention that it has created necessary manpower and infrastructure to implement Outcome Based Education from the year 2014-15. Today, JSSATEN has total student strength of over 4000, who are mentored by more than 250 Faculty Members. The Campus has finest accommodation for girls and boys. http://jssaten.ac.in/

ABOUT THE DEPARTMENT

Electronics Engineering Department stands tall amongst other branches of engineering disciplines. Commissioned in the year 1998, to offer graduate level programme in 'Electronics and Communication Engineering' , the Department has seen remarkable growth in terms of quality of student intake, inclusion of post-graduate programme Advance Electronics and Communication with specialization in VLSI Design' from 2008, applauding achievements of the students during and after graduation, faculty specialization and upgradation in several domain areas and infrastructure to provide the latest technical lab facilities e.g. Texas Instruments Centre of excellence and e-Yantra Laboratory Setup Initiative (eLSI) –IIT Bombay are unique facilities for research and project work, Entuple center of Excellence in the area of Microelectronics under cadence university programme. Department has consistently maintained an exemplary placement and academic record. B. Tech programme of Electronics and Communication Engineering accredited (Outcome Based Education) for two years by NBA from 1stJuly 2015. NBA approval program is a proof that department is committed to confidence and assurance on quality to all stake holders. Department has been identified as a research Centre in the field of electronics engineering for the technical university.
http://jssaten.ac.in/Academics/ECE/

AIM AND SCOPE

The focus of this FDP is on establishing an effective and efficient ecosystem for faculty and research scholars in the field of Analog Integrated Circuit Design domain. Strengthening faculty and research scholars skills will help in imparting good outcome based teaching and learning which in tern helps to provide better global level employment opportunities in top notch industries.
In view of this, department of Electronics and Communication Engineering will facilitate an opportunity by inviting eminent resource persons from renowned organizations. Also this FDP will empower skills in Electronic System Design and Manufacturing area for developing manpower to contribute towards Make-in India initiative.

COURSE CONTENTS

- **Analog Hardware Design and Interfacing Techniques**
- **Analog IC- Design Flow-CADENCE SUITE**
- **Electronic System Design and Manufacturing**
- **Electronic System Packaging**
- **Industrial Design of Electronic Products**
- **IC Design Hands on Session and Project Life Cycle**

RESOURCE PERSONS

- **Academic/Scientific Institutions**
  IITs, NITs,CDAC,DST,CDOT,NIC,DeITY etc
- **Industry Experts from**
  1. **Texas Instruments**
  2. **Synopsys**
  3. **ST Microelectronics**
  4. **NXP India**
  5. **Cadence**
  6. **Entuple Technologies**
  7. **NMTronics**

PARTICIPANTS

Faculty members of Engineering Colleges affiliated to AKTU and other Universities.
Research scholars & PG students pursuing research / project work in this field.

Technical Education Quality Improvement Programm-Phase-III
Dr. A.P.J. Abdul Kalam Technical University, Lucknow

FACULTY DEVELOPMENT PROGRAMME

On

Analog Integrated Circuit Design using Cadence Analog Design Flow

27 th August– 1st September, 2018

REGISTRATION FORM

Name:……

Designation:……

Department:……...

Institution/Organization……..……

Area of Specialization:……

Academic Qualification:……

Address……..……

……..……..……..……

……..……..……

E-mail:……..……..

Contact No.:……

NO Registration Fee

Declaration

The above information furnished is correct to the best of my knowledge and belief.

Signature of Applicant

Signature of HOD

Signature & Seal of Principal / Director